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DIFAR MULTIPLEXER-DEMULTIPLEXER SYSTEM, LATEST IMPROVEMENTS

BY ARTHUR DELAGRANGE

UNDERWATER SYSTEMS DEPARTMENT

1 MAY 1992

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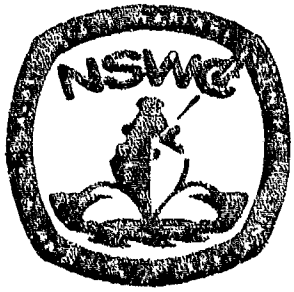

NAVAL SURFACE WARFARE CENTER

Dahlgren, Virginia 22448-5000 • Silver Spring, Maryland 20903-5000

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FOREWORD

This report describes the latest version of a multiplexer-demultiplexer system for DIFAR signals designed by the Center's U20 Division. Significant changes have been made since the system was last described (in NSWC TR 86-220). Theory, circuitry, and performance are provided. This report supersedes TR 86-220.

Approved by:

C. A. KALIVRETENOS, Deputy Head
Underwater Systems Department

ABSTRACT

This report describes the updated version of a multiplexer-demultiplexer system for DIFAR signals designed by the Naval Surface Warfare Center's Sensors and Electronics Division. Theory, circuitry, and performance are provided. This report also serves as a maintenance manual for the systems.

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ILLUSTRATIONS

BACKGROUND

Over the years, many DIFAR multiplexers and demultiplexers have been designed and built at the Naval Surface Warfare Center, White Oak. What started as an in-Branch project has grown to where over a dozen systems have been built, many of them delivered to other agencies. Over 100 demultiplexer cards have been built. Some significant changes have been made since the system was last described in 1986. This report documents the latest system modification. A complete description is included, obviating the need for the previous report.

INTRODUCTION

A DIFAR sonobuoy has an omnidirectional hydrophone (OMNI), a dipole effectively oriented along a (magnetic) North-South axis (N-S), and a dipole effectively oriented along an East-West axis (E-W). Before transmission over the radio link, the three signals are multiplexed as shown in Figure 1. The OMNI occupies baseband. The two dipoles are modulated by quadrature phases of a 15-kHz subcarrier. Note that this does not mean one dipole occupies the upper sideband and the other the lower (single sideband). Both dipoles occupy both sidebands; they are separable because they are in quadrature. A 15-kHz pilot tone is added as a phase reference necessary for the demultiplexer. A 7.5-kHz signal derived from the 15 kHz is added as a frequency reference to assist the demultiplexer in finding the 15-kHz signal. The 15-kHz subcarrier may have sideband lines close by which could be mistaken for the reference. The 7.5 kHz occupies a vacant portion of the spectrum and prevents this ambiguity. The function of the demultiplexer is to convert this spectrum back to three channels of baseband information. It does this by generating a local 15-kHz subcarrier locked to the received subcarrier, and using this local subcarrier to demodulate the dipole signals back to baseband. The OMNI is recovered simply by low-pass filtering.

Previously a multiplexer-demultiplexer combination could be made to meet specification (30-dB channel separation) only by tweaking one or the other. Thus, there was no guarantee that both were not bad by an equal and offsetting amount. With the new design, the two are calibrated by independent means and meet specification when used together, a good indication that both are correct. Also, some of the old demultiplexer cards would drift out of specification, particularly when the cards were wiggled in their connectors. This was attributed to a change in contact resistance changing the effective supply voltage on the card. The new modulator circuit has less power-supply sensitivity. It also eliminates cross coupling between gain and balance adjustments.

MULTIPLEXER OPERATION

A block diagram of the multiplexer is shown in Figure 2. The input signals are band-limited by low-pass filters to prevent frequency aliasing or noise around the 7.5-kHz pilot, should high-frequency components be present in the input signals. The dipole signals are modulated up in frequency by quadrature phases of 15 kHz. They are then summed together with the OMNI and the two pilot tones to form the composite signal. The composite signal is low-pass filtered, as square waves are used for the subcarriers and modulators, causing unwanted harmonic frequency components.

DEMULTIPLEXER OPERATION

A block diagram of the demultiplexer is shown in Figure 3. The OMNI signal is recovered by low-pass filtering. The dipole signals are translated to baseband by multiplying by quadrature phases of 15 kHz and low-pass filtering. The 15 kHz is obtained by tracking the 15-kHz pilot tone with a phase-lock loop (PLL). The PLL acts as a very narrow tracking filter, tracking the pilot in frequency and phase but filtering out the sideband information.

The PLL used is actually a double loop. A 15-kHz loop performs the function just described. A 7.5-kHz loop locks on to the 7.5-kHz signal, and performs the functions of acquisition and frequency reference. It cannot provide the phase reference by itself, as the relative "phase" between the 15-kHz and 7.5-kHz signals cannot be guaranteed. The 15-kHz signal applies the necessary phase correction to the 7.5-kHz loop.

The 7.5 kHz is first isolated by a narrow-band filter and then clipped. The detector in the 7.5-kHz loop is a digital frequency-phase comparator circuit triggered on the edges of the input signal and the reference (VCO, or voltage-controlled oscillator), respectively. The output of the frequency-phase comparator is applied to the 7.5-kHz integrator, which slews the VCO until the reference is the same frequency as the input and temporarily in phase. The average output of the circuit is linearly proportional to the phase difference of the inputs over a ± 360-degree range (see Figure 4a) when locked in frequency. This corresponds to ± 720 degrees at 15 kHz, so any possible phase correction may be applied by the 15-kHz loop without exceeding the linear range of the 7.5-kHz detector. The direct path around the integrator is necessary to provide loop damping.

Note that the 7.5-kHz loop is self-acquiring: if more transitions occur at one input than at the other, the comparator circuit remains in the corresponding state, slewing the integrator in the proper direction. Note also that with this detector, proper polarity must be observed. Overall feedback can be either negative, in which case the loop will acquire and track, or positive, in which case the loop will instead avoid the signal.

When the 7.5-kHz loop is locked in frequency, the 15-kHz loop by definition is also locked in frequency, but not necessarily in phase. An error voltage is developed at the output of the multiplier (modulator) proportional to the cosine of the phase difference (Figure 4b). This slews the 15-kHz integrator, which applies a bias to the 7.5-kHz integrator. The 7.5-kHz loop must then track at some phase difference other than 0 degrees to offset the bias. Polarity in the 15-kHz part of the loop is irrelevant, as with the multiplier detector either slope is available. If loop gain happens to be positive,

the VCO merely increases phase error until the stable slope is reached (settling time can thus vary widely depending on the initial phase error).

The system reaches equilibrium when the VCO matches both inputs in frequency, the 15-kHz reference is in quadrature with the 15-kHz input, and the 7.5-kHz reference is somewhere in the range -90 degrees to +90 degrees with respect to the 7.5-kHz input, depending on the relative "phase" between the incoming 15 kHz and 7.5 kHz.

If the 7.5-kHz loop is made much faster than the 15-kHz loop, operation of the two loops is essentially independent. The system tracks the 7.5 kHz but adjusts the phase of the 15 kHz. The requirements are that: (1) the inner loop be able to keep up with absolute frequency-phase changes of the 7.5-kHz signal; (2) the outer loop be able to keep up with relative "phase" changes between the 15-kHz and the 7.5-kHz signals; and (3) the latter occur much more slowly than the former. These requirements are all easy to satisfy.

CHANGES

The changes from the previous multiplexer design are: The modulator circuits have been changed, as the ones used previously sometimes were sensitive to supply voltage, having to be readjusted when changing supplies (a nuisance when debugging in a test fixture for later insertion into a rack), and also sometimes drifted and became noisy with age. The new ones are "home-built" with inverting amplifiers and switches. The N-S carrier feedthrough is balanced out simply by adding in an opposing signal from the clock (the E-W really does not matter, as subcarrier is added in anyway, but adjustment is much easier if this is nulled also). The summing network is rearranged; a transistor has been eliminated. The output filter has been changed and a phase correction network added. Phase linearity in the old unit was poor, causing dipole rejection not to meet specification at the higher signal frequencies.

It was found that the standard 4000 series of CMOS digital integrated circuits was too slow for the application. Switching times of supposedly opposite phases of a flip-flop could differ by a good part of a degree at 15 kHz, making the phases somewhat vague. It was replaced with the high-speed 74HC series, but this unfortunately will not take 15V, so supplies have been reduced to 6V. This lowers the performance of the op-amps, and some changes had to be made.

In the demultiplexer, the modulators have also been changed similarly. The balance in the 15-kHz loop (N-S modulator) is now done by using the offset adjustment of the integrating op-amp. Balance is not necessary in the E-W modulator. The input to the 7.5-kHz filter has been rearranged to eliminate the high-valued input resistor; part of the signal was actually coming in through stray capacitance! Center frequency adjustment is now by potentiometer rather than by adding a selected fixed resistor. The original single-stage active filter had been found to have insufficient rejection on the high side, and a passive LC low-pass was hastily added. The passive filter is now replaced with a second active stage. Gain of the three channels is now also adjusted by potentiometer rather than adding a selected fixed resistor; OMNI formerly was not adjustable at all. The VCO has been changed to use the same inductor as the filters. Some parameters in the loops have been changed for better stability.

MULTIPLEXER CIRCUITRY

Multiplexer circuitry is shown in Figures 5 and 6. The input filters are identical 5-pole low-pass filters having a cutoff frequency of 5 kHz. Each filter consists of a ladder of serious resistors and shunt active "D" elements (also called super-capacitors or frequency-dependent-negative-resistors) (Reference 1), terminated at each end with an inductor and capacitor. The inductor improves the filter characteristic by improving the usual capacitive termination (Reference 2). Zeros have been added at 7.5 kHz and 15 kHz by adding resistors in series with the super-capacitors. The filter characteristic is shown in Figure 7.

Balanced modulating is now done by creating an inverted signal in an op-amp inverter and switching between inverted and non-inverted signals by CMOS switches driven by opposing clock phases. The obvious way is to connect a pair of switches between the pair of op-amps and the filter. This does not always work. One switch may turn on before the other turns off, momentarily connecting the two op-amp outputs together. This creates a monster nonlinear transient which ruins performance. The filter input resistor (same as summing resistor) is positioned between the op-amps and the switches to prevent this (two resistors are now required). The N-S carrier feedthrough is balanced out by adding in an opposing signal from the clock. In theory, the E-W need not be balanced, as feedthrough only changes the amplitude of the pilot tone slightly, but in practice feedthrough tends to obscure the N-S component, so both are done. If the gain of the inverter amp is not exactly unity, some signal is left at baseband and adds to the OMNI. Using matched resistor networks as shown, this remnant is more than 30 dB down without adjustment, which is adequate. System-wise the dipole signals are always present in the OMNI anyway, so this amounts to a small gain error (less than 0.3 dB).

The 15 kHz is derived from a 60-kHz crystal oscillator by a divide-by-four shift register counter. The 7.5 kHz is generated from the 15 kHz by a divide-by-two counter. The CMOS logic clamps nicely to the power supply, giving a standardized voltage. The 7.5 kHz is bandpass filtered by an RLC, as its third harmonic would be within the band of the output filter.

The five signals are summed by a resistor network and low-passed by a 7-pole passive L-C ladder filter having a cutoff frequency of 25 kHz. The ladder is terminated at both ends by resistances, the summing network being the input termination. This arrangement prevents exceeding the slew rate of the output op-amp, which could cause asymmetrical distortion of the signal and hence unwanted phase shifts. A phase correction network is added at the output to improve phase linearity. The basic phase shift network using a shunt capacitor gives an arctangent curve, whose bend is opposite that of the filter. Thus overall phase shift is higher, but more linear. Amplitude is not affected. The series capacitor further improves phase linearity. It does boost the amplitude response at high frequency, but this actually helps, as the amplitude response of the filter sags a bit at the high end of the band. The resistor in series with the series capacitor limits its effect at frequencies above the range of

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1 Delagrange, A D., *An Active Filter Primer, Mod 2*, NAVSWC TR 87-174, 1 Sep 1987, Naval Surface Warfare Center, White Oak, Md

2 Delagrange, A D., *A Useful Filter Family*, NSWC/WOL TR 75-170, 20 Oct 1975, Naval Surface Weapons Center White Oak, Md

interest, reducing high-frequency gain, and hence noise. The output filter characteristic is shown in Figure 8. Across the information bands, amplitude must be constant and phase shift linear. Otherwise the sidebands are altered and the independence of the dipoles is lost.

Leftover sections from two matched resistor and one quad op-amp ICs (Integrated circuits) have been used to provide an overload indication. This is particularly important now with the reduced dynamic range due to the lower power-supply voltage. Overloading causes nonlinearity, destroying the independence of the dipoles.

DEMULTIPLEXER CIRCUITRY

The multiplier in the 15-kHz PLL (Figure 9) is actually the N-S balanced modulator of the demultiplexer. For the proper combination of input frequencies and output filtering, a balanced modulator acts as a linear multiplier; that is the case here. This has the advantage that the gain in the 15-kHz loop, and hence the loop parameters, do not vary with modulation level or power-supply voltage. The disadvantage is that they do vary, however, with input carrier amplitude. The input buffer is unity gain and assumes a 15 kHz carrier level of 100mVRMS (the 7.5-kHz carrier level should be roughly equal to the 15-kHz).

The 15-kHz integrator is zeroed by the op-amp balance; imbalance would cause the loop to track with a phase error. If the input signal is removed for a long time, the integrator will drift off and saturate. It could then reacquire too near the edge of its range. Therefore, a hi-lo threshold detector senses if the integrator exceeds the center 60% of its range. If this occurs, forward bias is momentarily applied to a field-effect transistor which discharges the feedback capacitor, returning the integrator to the center of its range.

The 7.5-kHz filter consists of two stages, each consisting of an op amp with a bridged tee as the feedback path. Near the resonant frequency the gain of the bridged tee is low, so the overall filter gain is high. A trimming potentiometer is adjusted to peak the output at 7.5 kHz (adjustment is actually done by setting the stage to 180 degrees phase shift, which is a more sensitive method).

A comparator clips the 7.5-kHz signal. Hysteresis is necessary to prevent extraneous zero crossings from noise, as the 7.5-kHz detector will not tolerate these. Hysteresis normally causes phase shift. This is not tolerable here because it is amplitude-dependent, so if carrier amplitude varies (fading channel), phase shift is introduced--possibly at a rate faster than the 15-kHz loop could compensate. Previously the positive feedback was AC-coupled with a short time constant to avoid this. When 16 cards were crammed into a single rack, it was found that for a channel with no signal the clipper would attempt to clip whatever noise appeared at its input, and the resultant garbage introduced noise into the output of adjacent cards. In the new design the positive feedback is DC-coupled but one-sided. As amplitude changes the output negative transition moves but not the positive transition, *i.e.*, duty cycle changes. However, the 7.5-kHz loop senses only the positive transitions, so this is satisfactory. When the input signal is below the hysteresis level the clipper simply latches up in one state, generating no noise.

The 7.5 kHz detector circuit operates thusly: a positive transition on either input sets that particular flip-flop. It stays set until the other flip-flop gets set. An "AND"

gate senses this condition and immediately resets both flip-flops. Thus one flip-flop output corresponds to a "faster" pulse and the other to a "slower" pulse, and the two are mutually exclusive. If the input frequency is higher than the VCO frequency, pulses occur only from the "faster" flip-flop, slewing the integrator to raise the VCO frequency. No pulses occur at the "slower" output (except for a very narrow spike during the reset). The reverse occurs if the VCO frequency is higher. If the frequencies are the same but the input leads the VCO in phase, a "faster" pulse will occur each cycle beginning at the input transition and ending at the VCO transition, reducing the phase lag of the VCO. Again, the reverse happens if the VCO leads. Because the circuit works over a range of ±360 degrees, the definition of which signal leads depends on the history of events. This is not relevant in this application, as the loop settles to 0 degree phase difference (excluding bias from the 15 kHz loop). The output of the detector circuit is differential, but the flip-flops also have a complement output, so this is used for one and the two are then simply added to avoid using a differential integrator. CMOS logic clamps nicely to the power supply and ground, inherently providing pulses of standardized voltage.

The 7.5-kHz integrator has a resistor in series with the feedback capacitor to effect the necessary direct path for loop damping. This resistor is bypassed with a capacitance chosen to block the AC signals while, it is hoped, not affecting the loop response significantly (the 15-kHz integrator does not require this resistor because the 7.5-kHz loop is so much faster that it provides the damping). The 7.5-kHz integrator need not be balanced precisely, as the 15-kHz loop adjusts the phase anyway.

The integrators have capacitors to ground on the outputs. Both are coupled to switching circuits, and the transients were driving the op-amps crazy. In addition, any noise at the input to the VCO causes unwanted modulation, which in turn produces noise in the dipole outputs. The 356 op amps previously used are not guaranteed stable for large capacitance loads, and some were found to oscillate when used with the lower supply voltage. The 3160s are not guaranteed either, but they seem to put up with it.

The VCO is an LC oscillator to minimize jitter. An op amp provides the necessary gain; a DC bias path ensures that the op-amp cannot latch up in a saturated state. The capacitance is controlled by varying the voltage across a back-biased diode. The oscillator runs at 60 kHz. A divide-by-four shift-register counter gives quadrature phases of 15 kHz. A divide-by-two triggered from an arbitrary phase of the 15-kHz gives the 7.5 kHz.

A second balanced modulator driven in quadrature from the first detects the 15-kHz carrier when the loop is locked on. An averager and comparator give a lock indication when the rectified and averaged signal exceeds a preset threshold. Note that this indicates only that the loop is locked in frequency; it may or may not have settled to the necessary phase accuracy yet.

A second comparator gives an overload indication if the input exceeds a second threshold, indicating too much amplitude modulation on the carrier. The indicator is set to come on somewhat before overload actually occurs.

The output filters (Figure 10) are the same as the ones used at the multiplexer inputs. The dipole signals are taken from the two balanced modulators; the OMNI comes directly from the input buffer. The inductor has an additional advantage here in that it prevents the slow filter op-amps from being driven into nonlinear operation by the

high frequency components of the balanced modulator outputs by slowing the fast-rise steps. To achieve maximum dynamic range with the new lower supply voltage, CMOS op-amps have been used. The outputs swing "rail to rail," but they have a relatively high output impedance. They can drive only about three 3 feet of 50-ohm cable without oscillating. The compensation network added at the outputs extends this to 10 feet, which is adequate in most cases.

LOOP ANALYSIS

It is necessary to analyze the loop as a feedback system to predict its dynamic behavior. Methods similar to those of Reference 3 may be used and flow-graphs (Reference 4) are of help. A block diagram and corresponding flow graph of the double loop are shown in Figure 11. All transfer functions are written in terms of phase at 7.5 kHz. Note also that the gain of the 15-kHz detector differs from that of the 7.5 kHz detector by a factor c, which depends on the types of detectors, and also on subcarrier input amplitude.

Only the poles (roots of the denominator) of the transfer function need to be determined for stability analysis. The flow graph may be simplified by combining parallel branches and ignoring inputs and outputs, as shown in Figure 12a. The poles occur when the loop gain is equal to +1. The polynomial is found to be:

$$s^3 + K_0K_V d\, s^2 + K_0K_V\left(\frac{1}{\tau_1} + \frac{2cd}{\tau_2}\right)s + 2c\frac{K_0K_V}{\tau_1\tau_2} = 0$$

This indicates a third order system.

The roots of this polynomial can be found, but the expressions are hopelessly involved. Instead, assume that the 15-kHz integrator is enough slower than the 7.5-kHz integrator that at the natural frequency of the 7.5-loop the gain of the 15-kHz integrator is much less than unity so it does not add a significant contribution. The 7.5-kHz loop alone is shown in Figure 12b. The poles are found to be:

$$s = \frac{-K_0K_V d \pm \sqrt{(K_0K_V d)^2 - 4\frac{K_0K_V}{\tau_1}}}{2}$$

3 Gardner, *Phaselock Techniques*, Wiley, 1966

4 Mason and Zimmerman, *Electronic Circuits, Signals, and Systems*, Wiley, 1960

The 7.5-kHz loop behaves like a normal second-order loop. For reasonable values the poles are a complex pair with natural radian frequency:

$$\omega_n = \sqrt{\frac{K_\phi K_V}{\tau_1}}$$

and a damping ratio:

$$\zeta = \frac{d}{2}\sqrt{K_\phi K_V \tau_1} = \frac{d}{2}\omega_n \tau_1$$

(The usual equations).

The poles of the 15-kHz loop are now found as follows. The transfer function of the 7.5-kHz loop along the branch common to both loops is found. This function is evaluated for S→0, because the 7.5-kHz loop is operating far below its natural frequency. The result ($-1/K_\phi$) is substituted for the upper loop (figure 12c). The 15-kHz loop is then found to have a single real pole at:

$$S = -\frac{2c}{d}$$

The 15-kHz loop behaves like a simple first-order system having a time constant:

$$T = \frac{2}{2c}$$

The speed of the 7.5-kHz loop removes the effects of the integrating VCO, so one detector simply adjusts the other and the only factors that matter are the relative gain and the 15-kHz integrator time constant.

DERIVATION OF LOOP PARAMETERS

The circuit parameters are found as follows: the time constant of each integrator is the product of the input resistor and the feedback capacitor (1 MΩ x 1 μf = 1 sec for the 15-kHz integrator and 0.5 MΩ x 0.01 μf = 0.005 sec for the 7.5-kHz integrator). The previous report treated the circuit as having a differential input integrator with twice the time constant. The new analysis treats the detector as having a 0V to +6V output into a 0.5-megohm equivalent resistance. The resulting answer is the same for the 7.5-kHz loop bandwidth, but there was an error in the damping ratio calculation and another in the 15-kHz loop analysis. However, in the previous report yet another error was made which canceled: a factor of two was assigned to both the 15-kHz detector and the 15-kHz output of the VCO, which was redundant! The direct path gain added to the 7.5-kHz integrator is the ratio of the feedback resistor to the input resistor, 100 kΩ / 0.5MΩ = 0.2.

The phase detector characteristic is the average (DC) voltage out of the detector versus the phase difference between the inputs; the phase detector gain is the slope of

this curve at the point of loop equilibrium. The 7.5-kHz detector changes linearly from 0V to 6V in 4π radians, so the gain is 6V / 4π everywhere. The 15-kHz phase detector outputs for 0 and π/2 rad phase difference inputs are shown in Figure 13. It is not immediately obvious, but the average value varies sinusoidally, shown in Figure 4b. To see that the detector characteristic is indeed sinusoidal, recall that the balanced modulator multiplies a sine by a square wave, which can be represented as a sine wave plus harmonics. Only the fundamental will contribute to the DC component, so we essentially have the product of sinusoids. This generates only more sinusoids, and the term with nonzero average will be sinusoidal in phase difference. The maximum occurs at 0 rad where the waveform is a full-wave-rectified sine wave (Figure 13a). The average of this waveform of unit amplitude is 2/π, found by integrating the sinusoidal peaks. At π/2 rad (see Figure 13b) the average is clearly 0; this is where the loop will stabilize. The slope of a unit sine wave at the origin is unity. The peak of a 1-vRMS sine wave is $\sqrt{2}$V. The N-S filter attenuates the signal by one half. The detector gain is therefore $(0.1)(2/\pi)(\sqrt{2})/2 = 0.045$ V/rad.

The VCO gain must be found experimentally. The loop is made to track 7.4 kHz and 7.6 kHz and the respective 7.5-kHz integrator output voltages noted. The VCO gain is then $2\pi(200)/\Delta V$. The VCO measured was 1172 Hz/V. There is some variation due to the variable capacitors, but it is not significant.

The parameters of the loop are then:

$K_0 = 6V/4\pi$ rad $= 0.48$V/rad

$K_V = 1172$ Hz/V $= 7366$ rad/V sec

$d = 0.2$

$t_1 = 0.005$ sec

$t_2 = 1$ sec

$c = (0.045\text{V/rad}) / (0.48\text{V/rad}) = 0.094$

Substituting:

$n = 840$ rad/sec $= 133$ Hz

$\delta = 0.84$

$T = 5.3$ sec

This is in fair agreement with experiment. In the approximation used above, the natural frequency and damping ratio are not affected by the capacitor across the feedback resistor in the 7.5-kHz integrator. Although not included in the analysis, in practice it is critical. It must be made as large as possible to minimize jitter in the VCO. However, this tends to bypass the damping resistor, reducing stability. Reducing the damping resistor value reduces the effect, but that in itself directly lowers the damping ratio. The values used were found experimentally to be optimal.

PERFORMANCE

The demultiplexer expects a level of 100 mVRMS (-20dBV) for each subcarrier. At about 10 dB below this the lock indicator light goes out, although the demultiplexer is still working. At 20 dB below the desired level the loop is still tracking, but the phase error is serious. Should the levels happen to be higher than expected, performance actually improves, as long as the overload indication is not on. As mentioned, the overload light is set to come on slightly before clipping, so if the light flashes occasionally the system is still working. The loop will still track if overloaded, but there can be phase error due to the nonlinearity from clipping.

Figure 14 shows the performance as noise is added to the demultiplexer input signal. The subcarrier level was kept constant. A 1-VRMS 1-kHz sine wave was put on the OMNI and N-S. Noise of 20-kHz bandwidth was added to the composite signal. Output SNR was taken as the ratio of the signal at the N-S output to the extraneous signal plus noise at the E-W output. Input SNR was taken as the ratio of one subcarrier to the total input noise; it could also be represented as the ratio of the input signal to the noise by adding 20 dB to each of the numbers on the horizontal scale.

Figure 15 shows the crosstalk between the two dipole channels. The two dipoles behave differently because the 15-kHz phase pilot is not at 45 degrees between the two. Note that at maximum input amplitude the rejection is not as good as it should be, although it passes easily at lower amplitude. This is a reminder that, although analysis by linear approximation gives pretty good results, the system is actually nonlinear. In some cases the output feedthrough is actually at double the input frequency. Note also that in some cases the error applies to the entire signal, not just the offending line, because the loop is tracking at the wrong phase. On the other hand, this problem does not apply to transients, as when the system wanders astray it does so with the slow (5-sec) time constant of the 15-kHz loop, so it does not react appreciably to short signals. Figure 16 gives the crosstalk between the OMNI and the dipole channels. Here there is little difference between the two dipoles, and amplitude does not matter.

Figure 17 shows the error between dipole channels, both phase and amplitude, for a multiplexer-demultiplexer pair picked at random. Phase error translates directly to DIFAR bearing error. An amplitude error of 0.3 dB translates to 1 degree bearing error, worst case. The errors become worst at the band edges, due to mismatch of the filters in the two channels. Figure 18 similarly shows the errors between one dipole and OMNI. Phase nonlinearity in the multiplexer output filter introduces error here.

POWER REQUIREMENTS

The multiplexer uses ±6V supplies at 40 ma. The demultiplexer uses ±6V at 50 ma (excluding indicator lights). Power supplies should be within ±15 mV. Card adjustment procedures are given in the appendices.

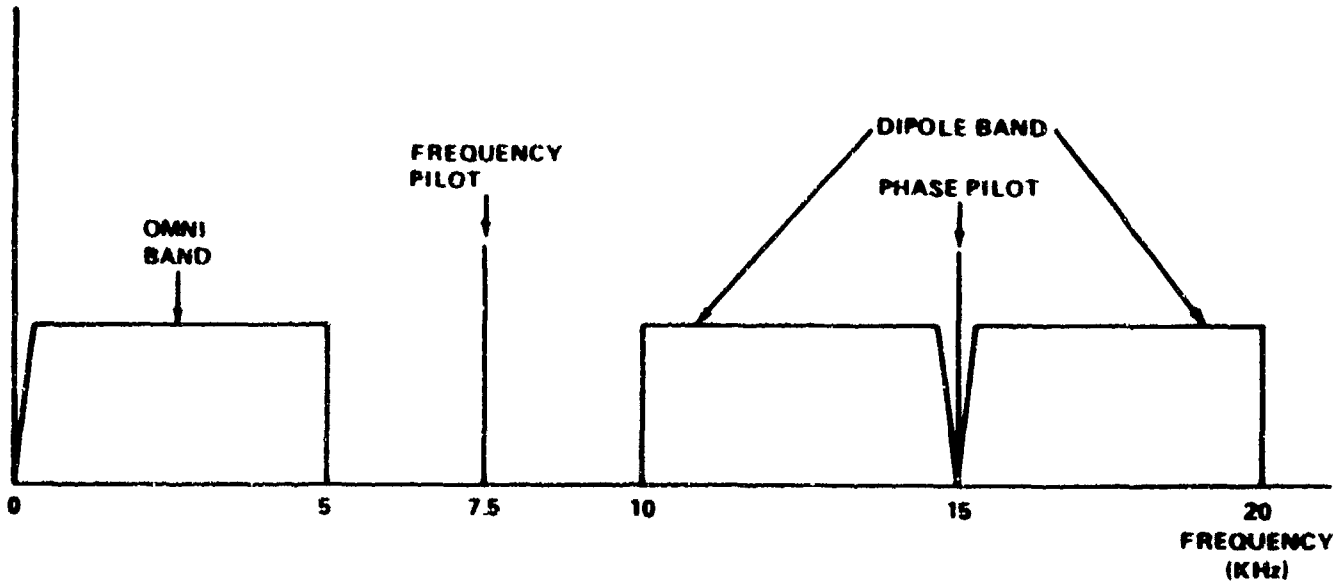


FIGURE 1. SPECTRUM OF MULTIPLEXED SIGNALS

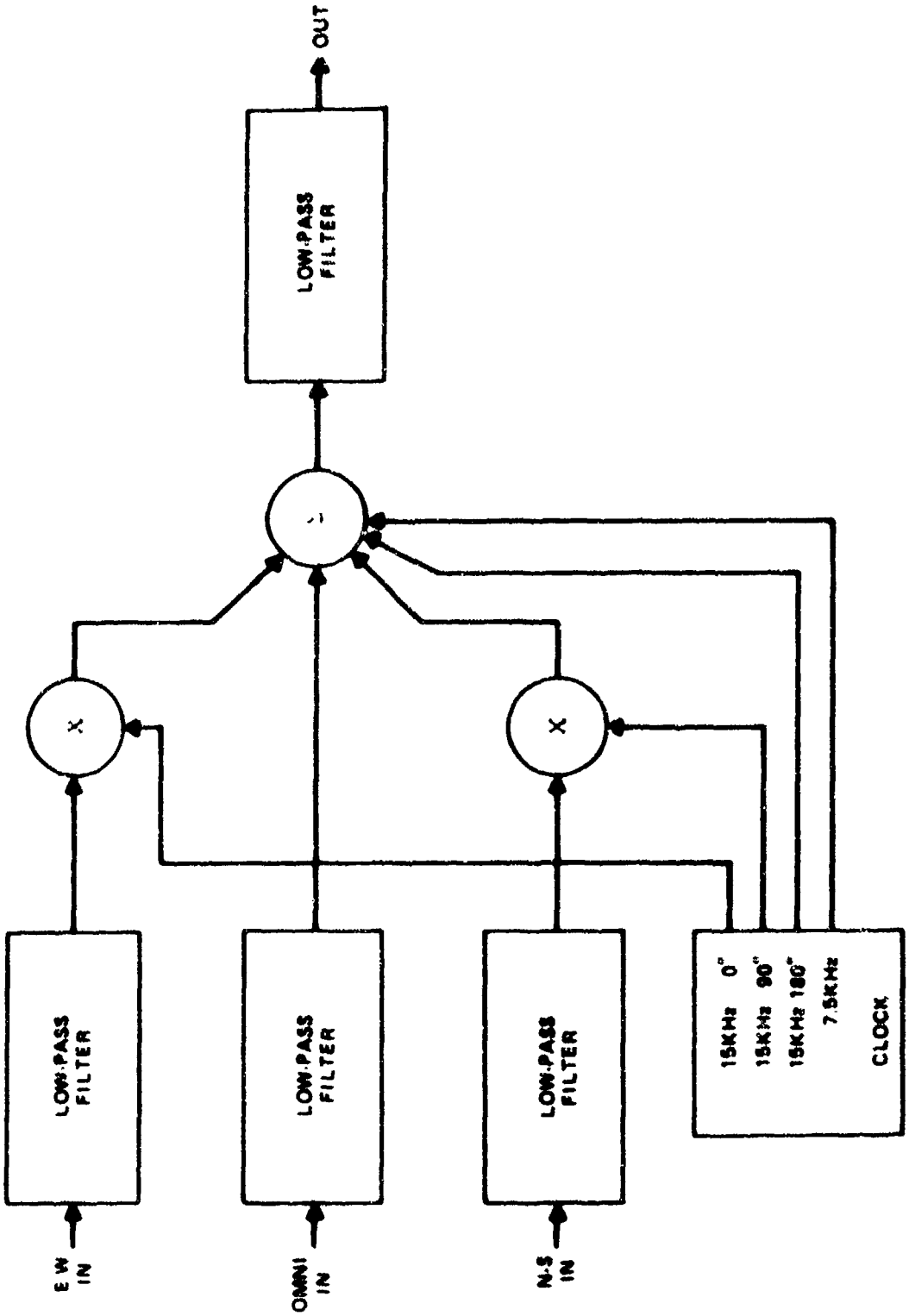


FIGURE 2. MULTIPLEXER BLOCK DIAGRAM

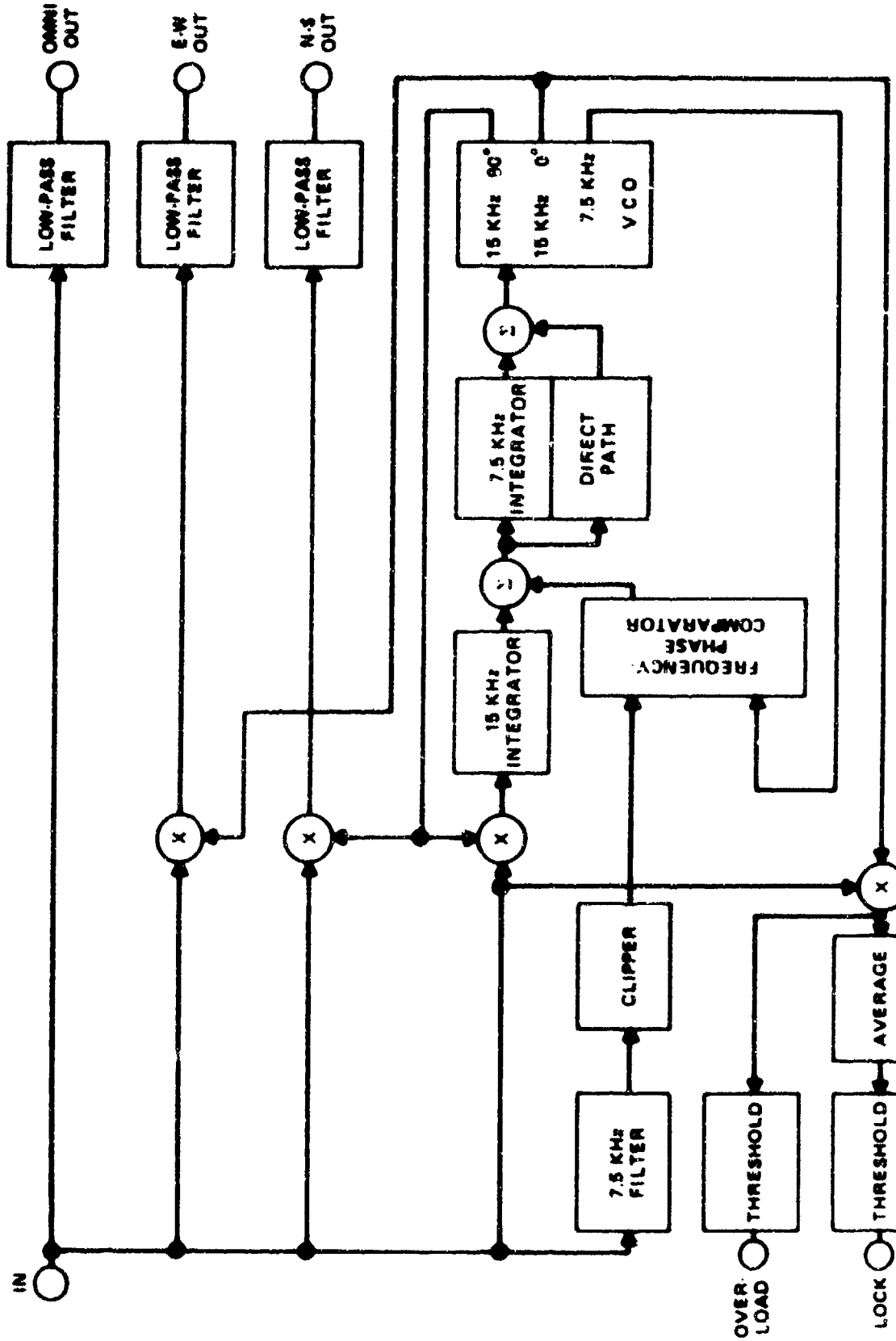
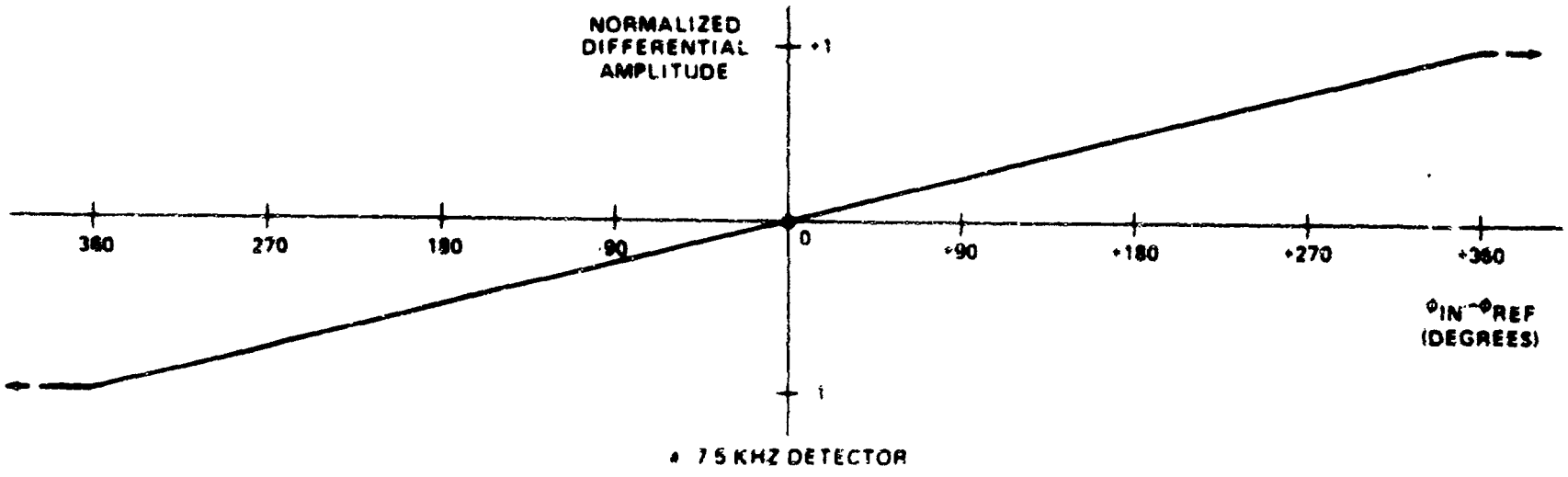
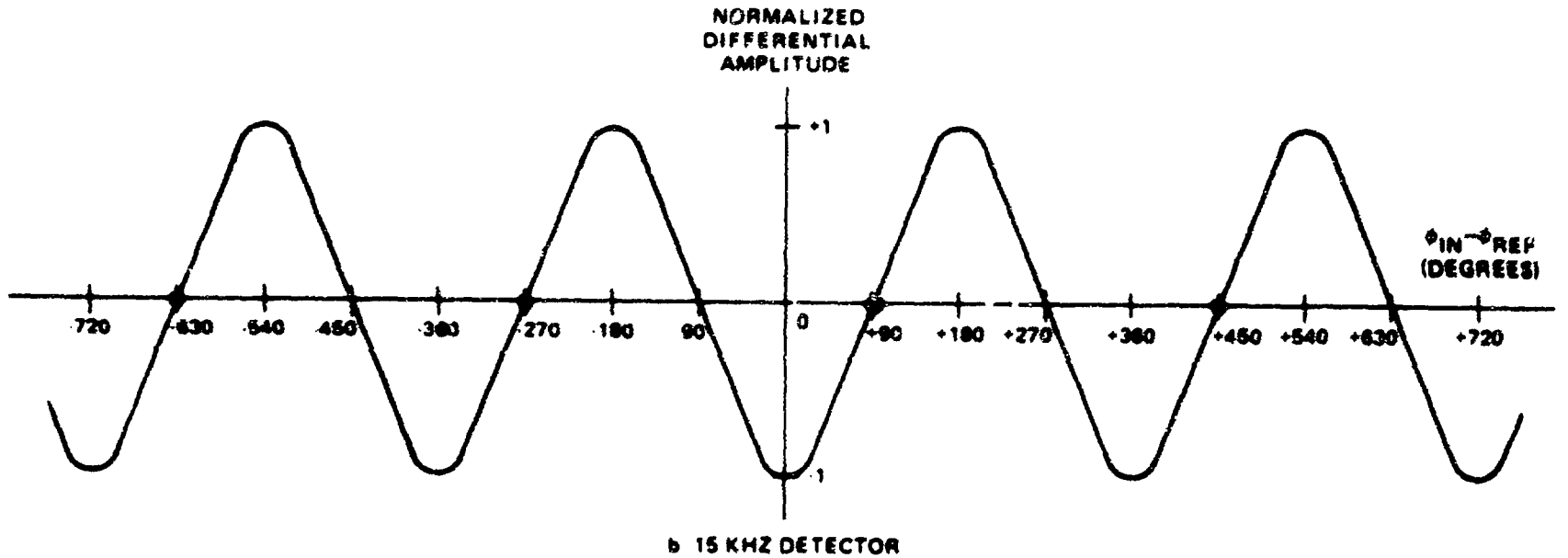


FIGURE 3. DEMULTIPLEXER BLOCK DIAGRAM



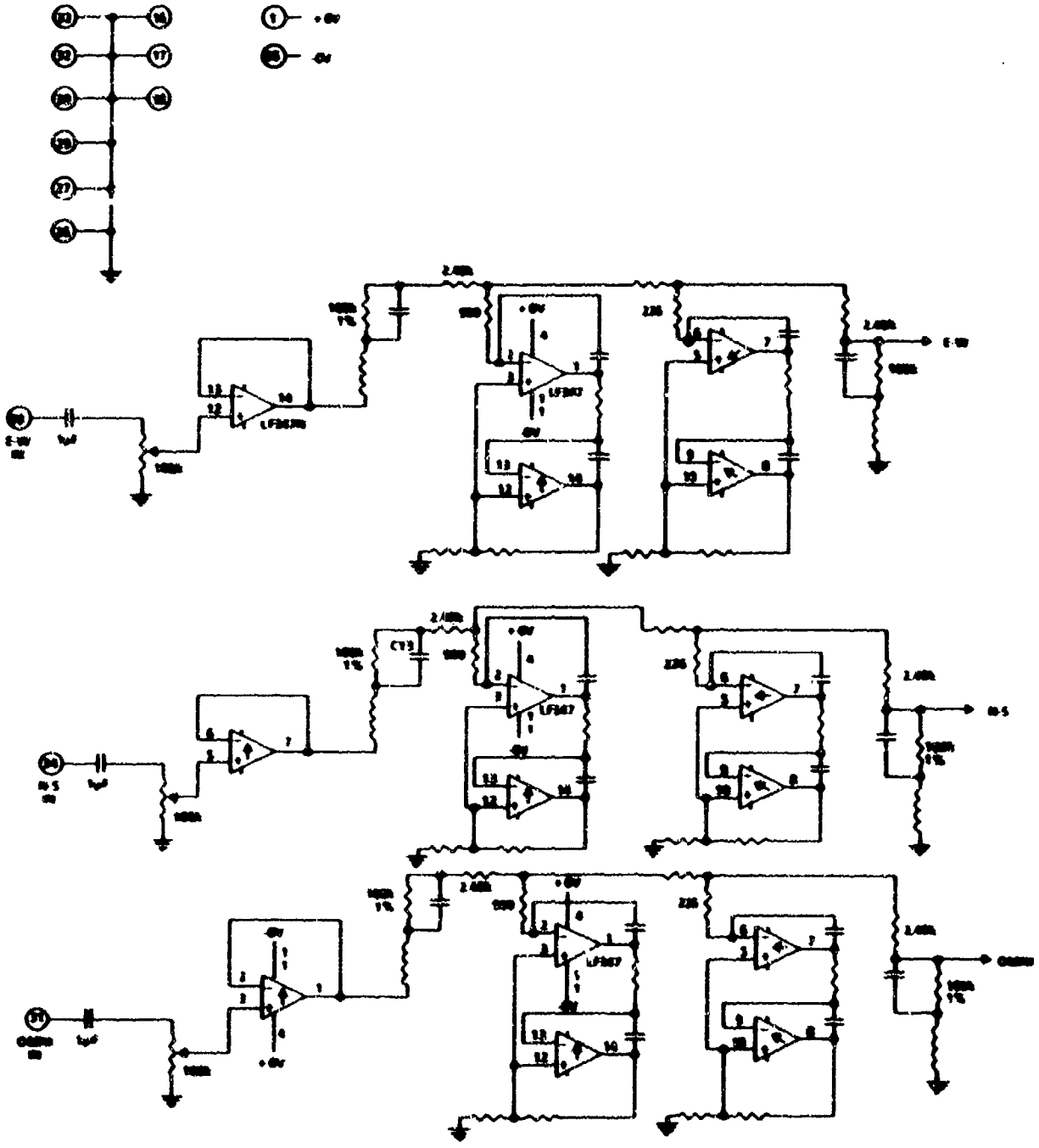
a 7.5 KHZ DETECTOR

NOTE: DOTS ARE
EQUILIBRIUM POINTS



b 15 KHZ DETECTOR

FIGURE 4. PHASE DETECTOR OUTPUTS



NOTES:

UNMARKED RESISTORS	4.99 kΩ 1%
UNMARKED CAPACITORS	0.01 μF 1%
UNMARKED INDUCTORS	68 mH

FIGURE 5 MULTIPLEXER INPUT FILTERS

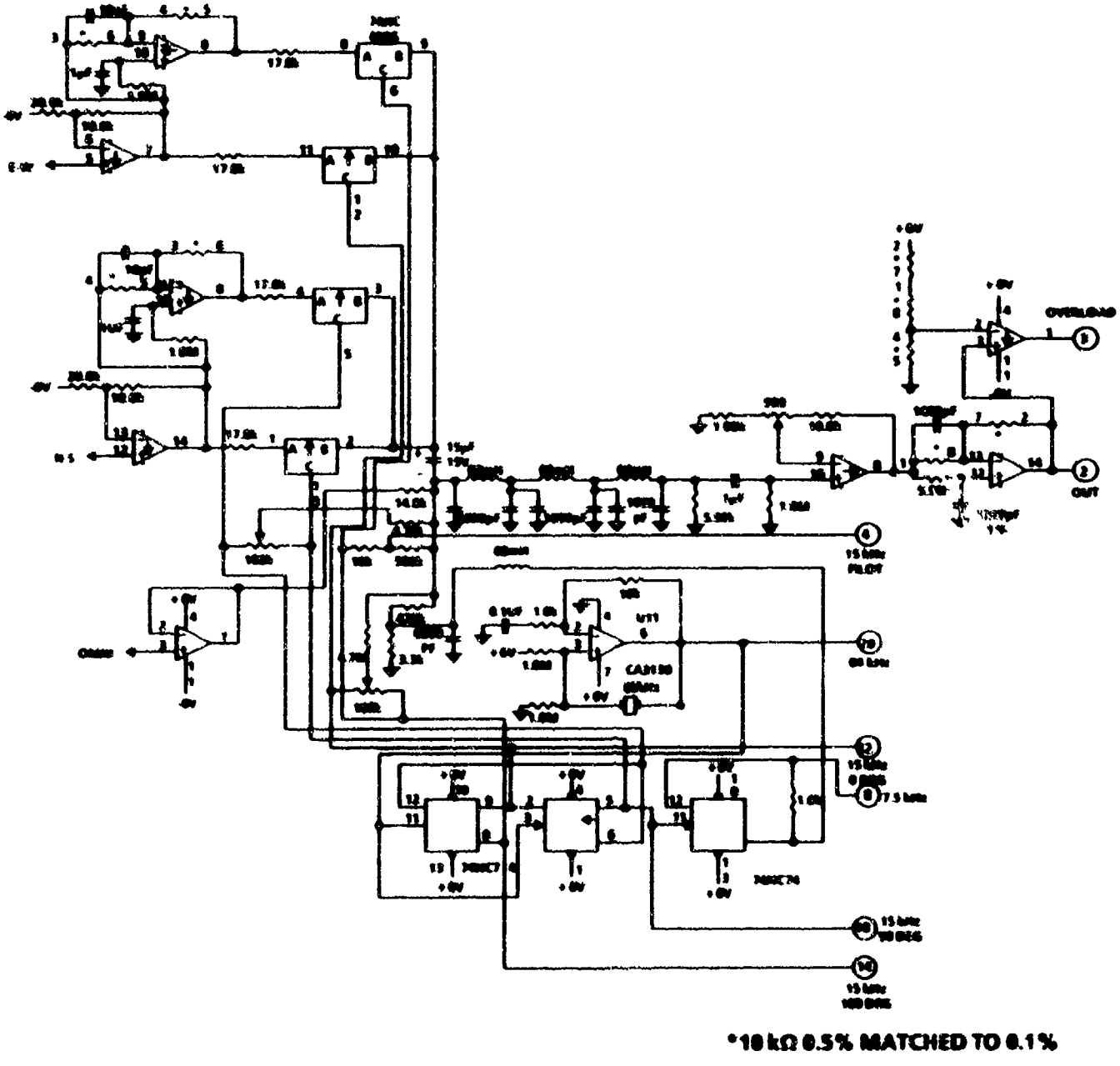


FIGURE 6 MULTIPLEXER SUMMING CIRCUIT

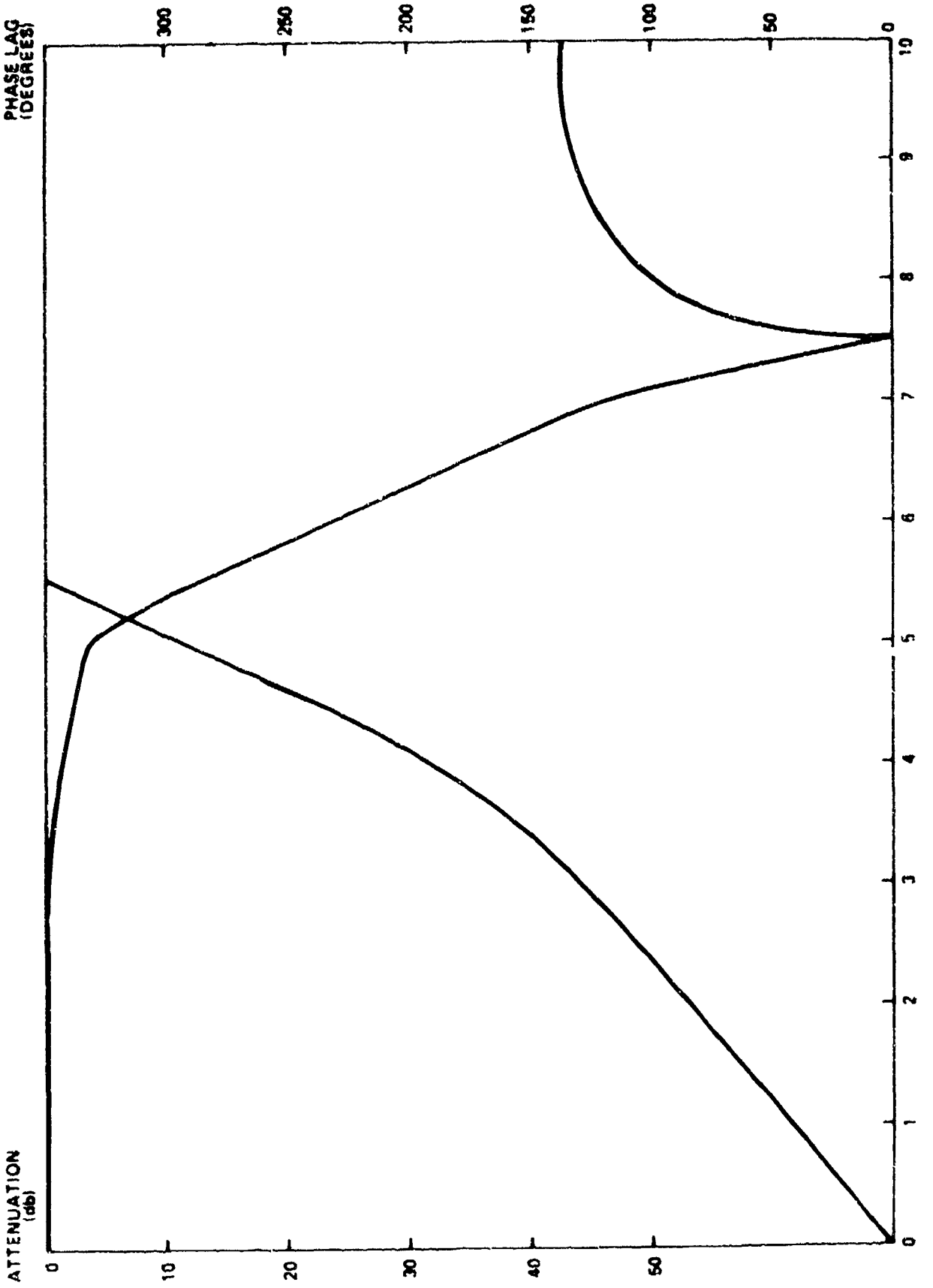


FIGURE 7. MULTIPLEXER INPUT FILTER CHARACTERISTICS

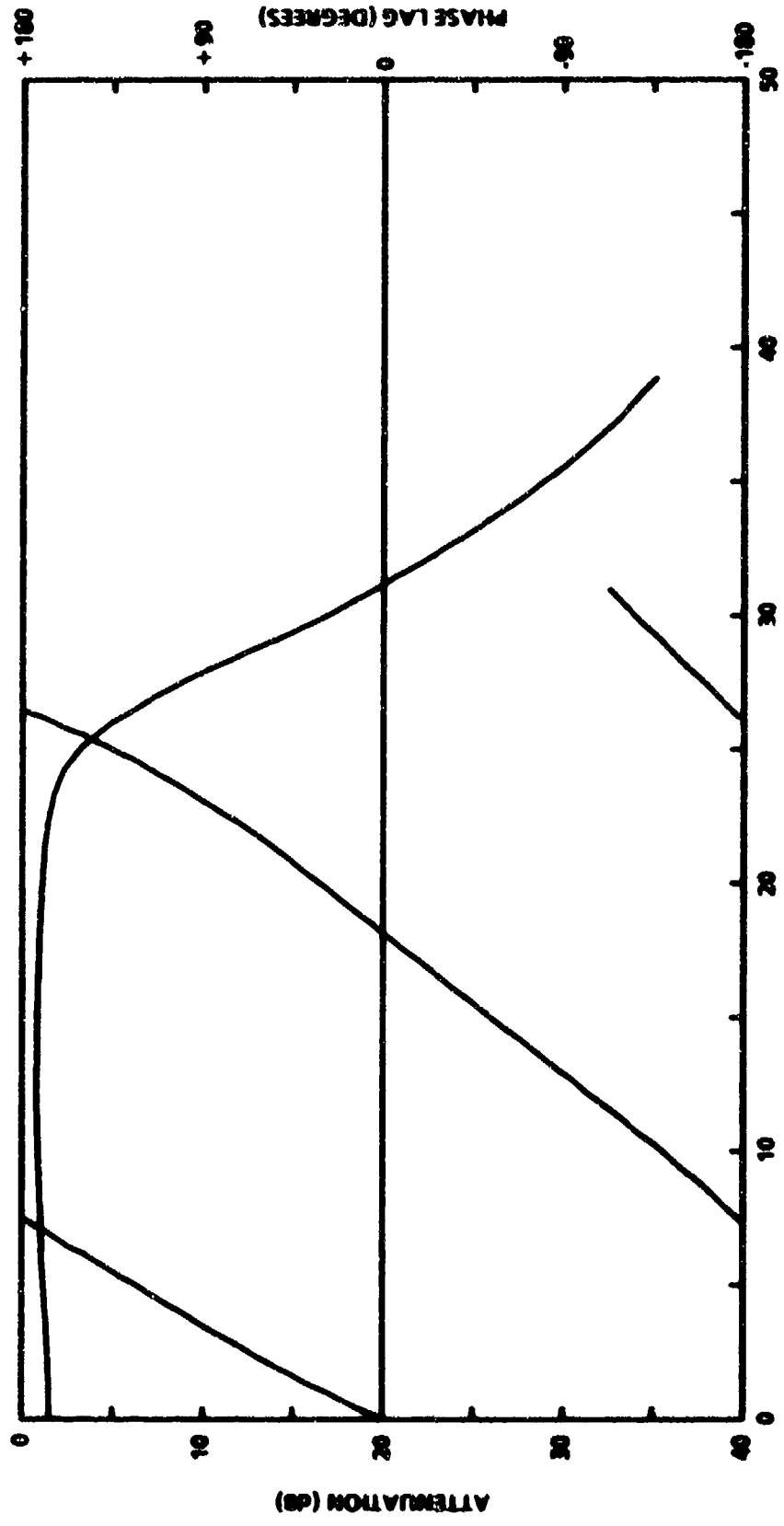


FIGURE 8. MULTIPLEXER OUTPUT FILTER CHARACTERISTICS

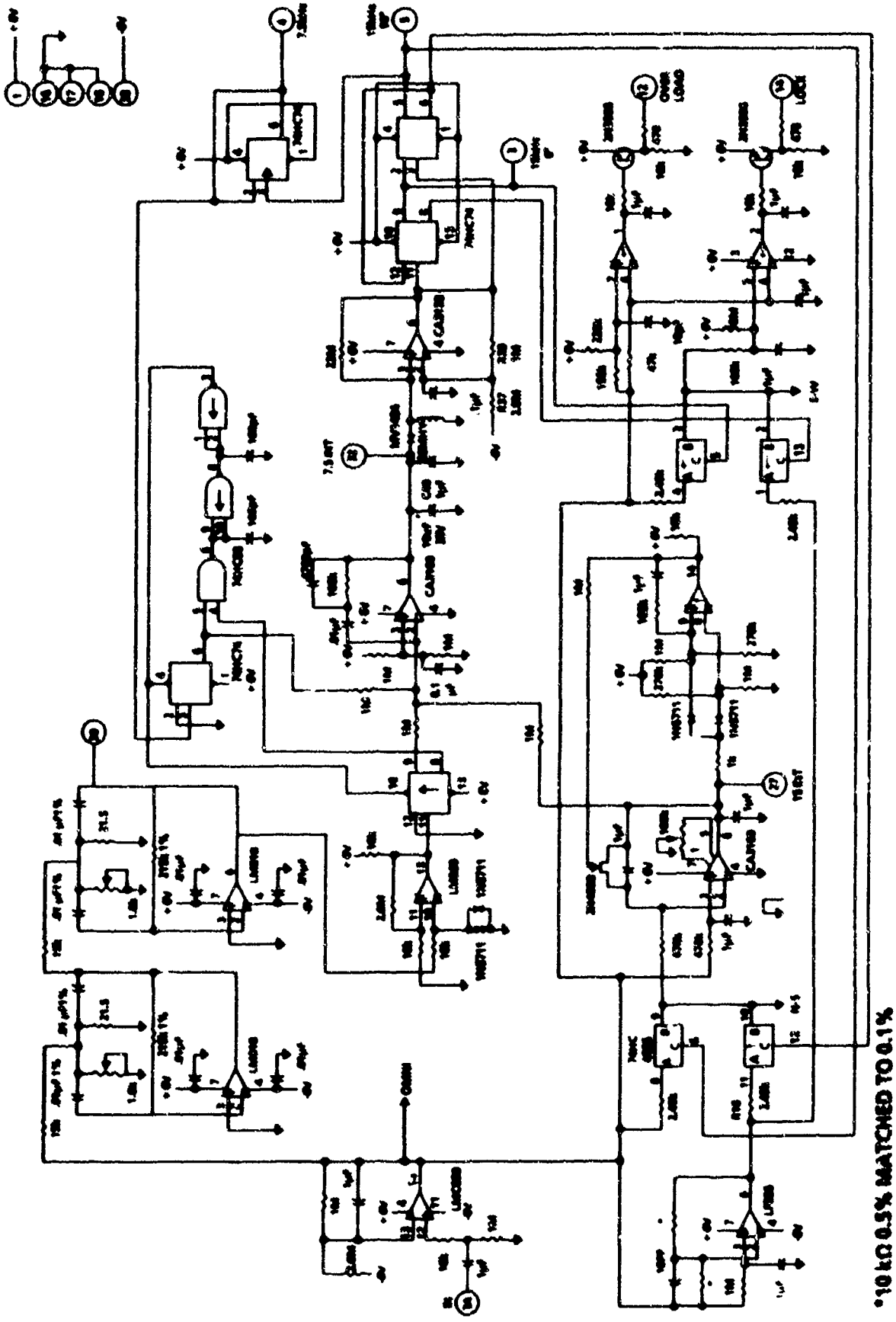
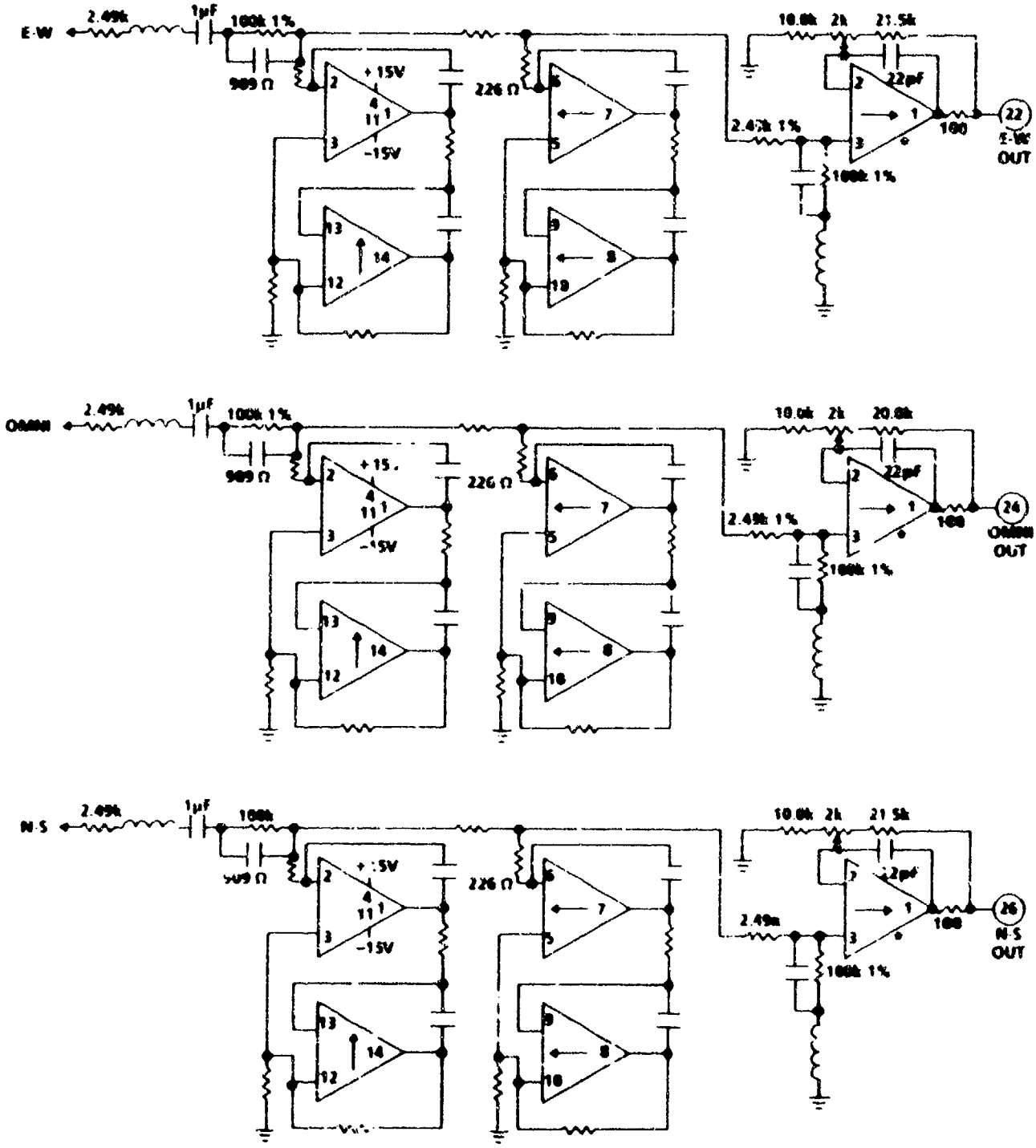


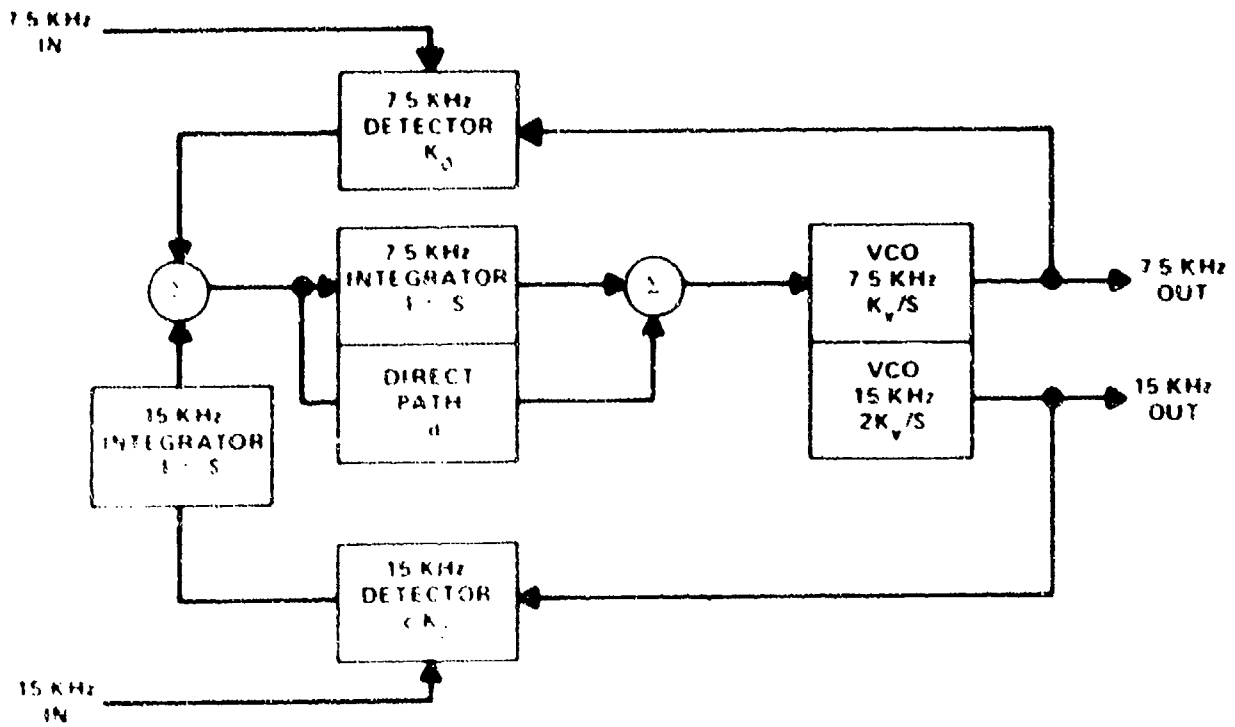
FIGURE 9. DEMULTIPLEXER PHASE-LOCK LOOP CIRCUIT

*10 kΩ 0.5% MATCHED TO 0.1%

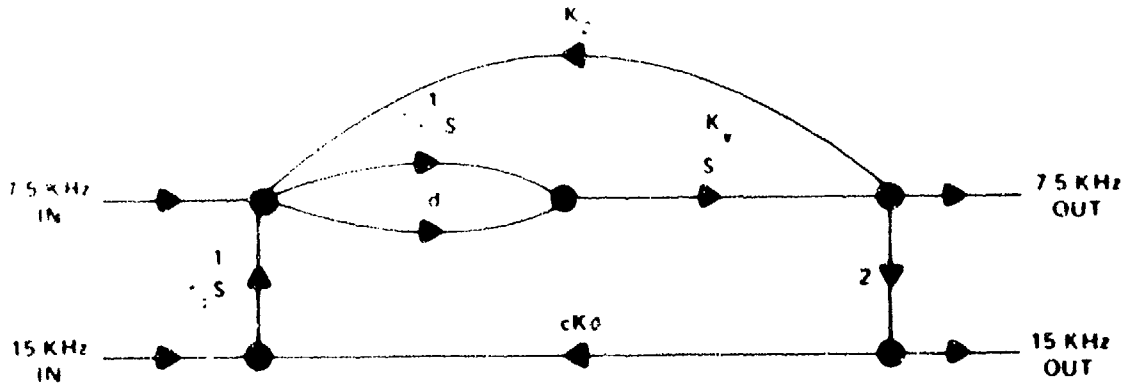


NOTES: UNMARKED CAPACITORS .01 1%
UNMARKED RESISTORS 4.99k 1%
ALL INDUCTORS 68 MHY
ALL OP AMPS LF 347 EXCEPT * LMC 660

FIGURE 10 DEMULTIPLEXER OUTPUT FILTER CIRCUITS

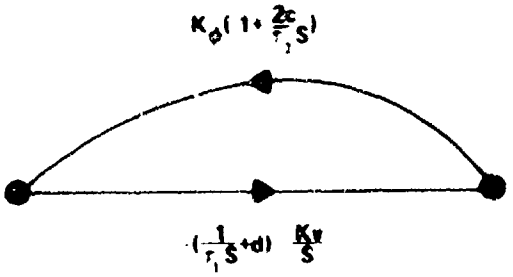


a BLOCK DIAGRAM

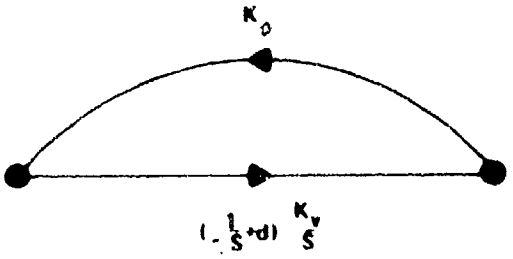


b FLOW GRAPH

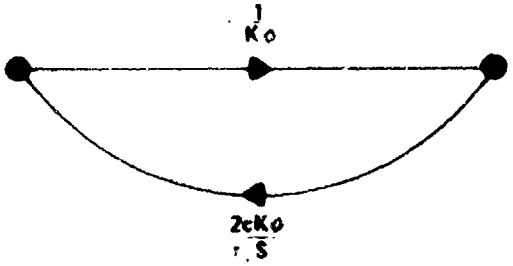
FIGURE 11. LOOP ANALYSIS



a DOUBLE LOOP

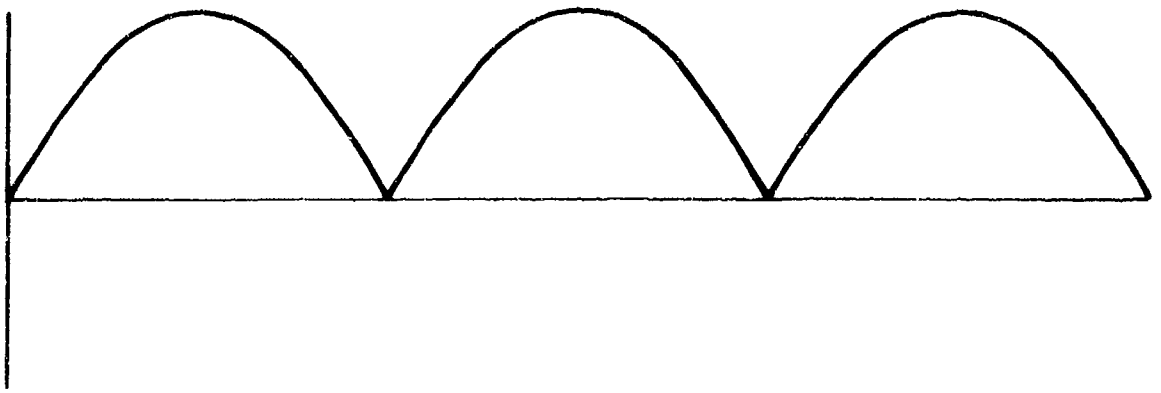


b 7 5 KHz LOOP

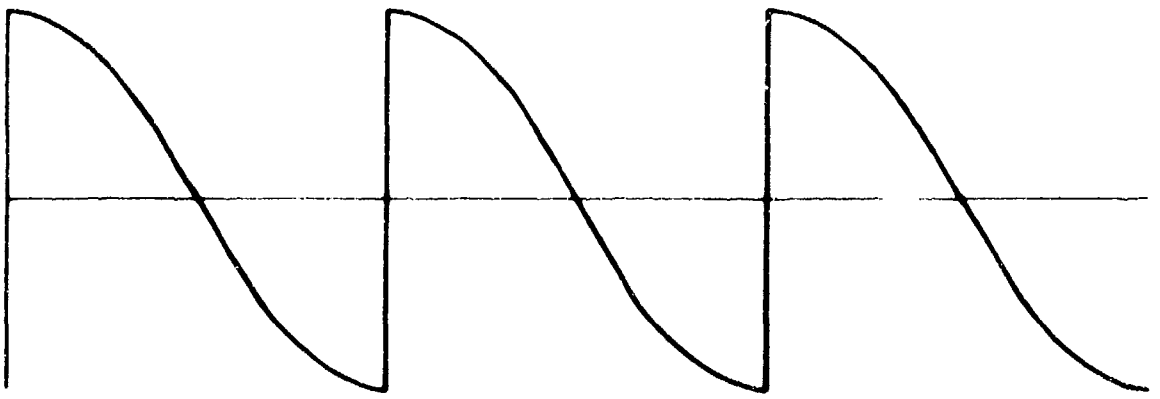


c 15 KHz LOOP

FIGURE 12 SIMPLIFIED FLOW GRAPHS



a ZERO PHASE DIFFERENCE



b π/2 RAD PHASE DIFFERENCE

FIGURE 13. BALANCED MODULATOR WAVEFORMS

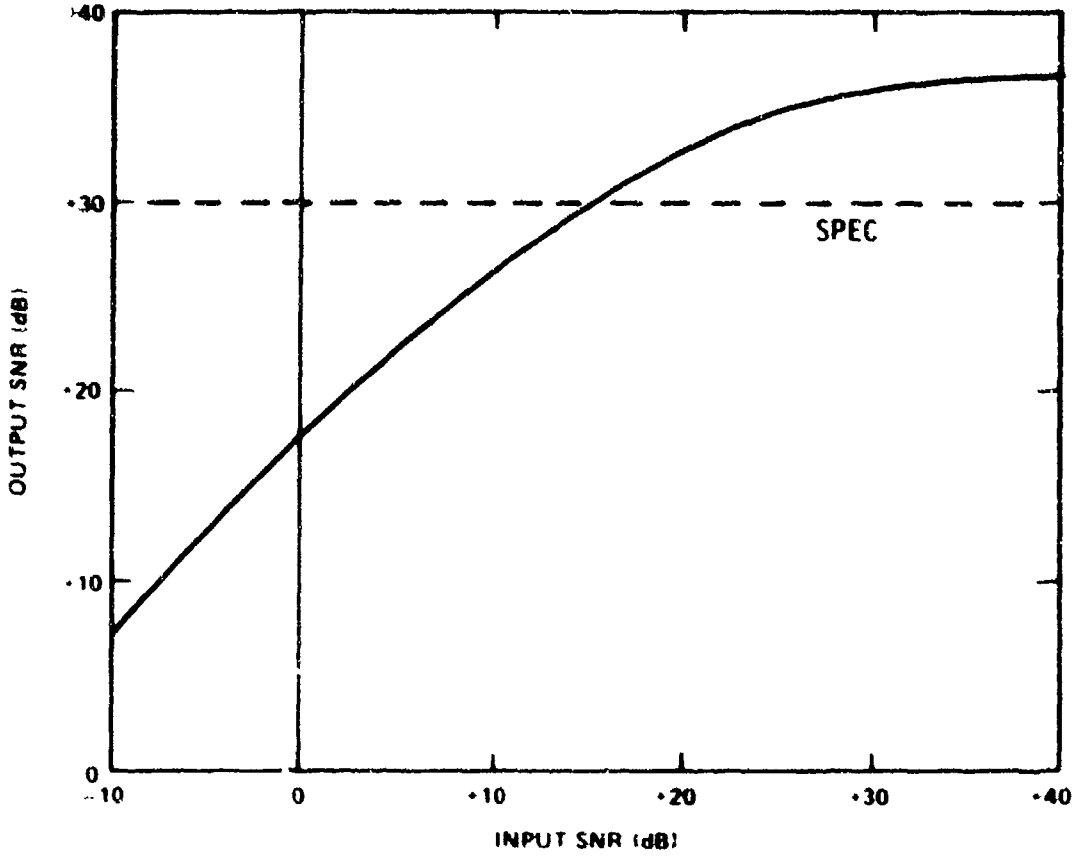


FIGURE 14. EFFECT OF NOISE AT DEMULTIPLEXER INPUT

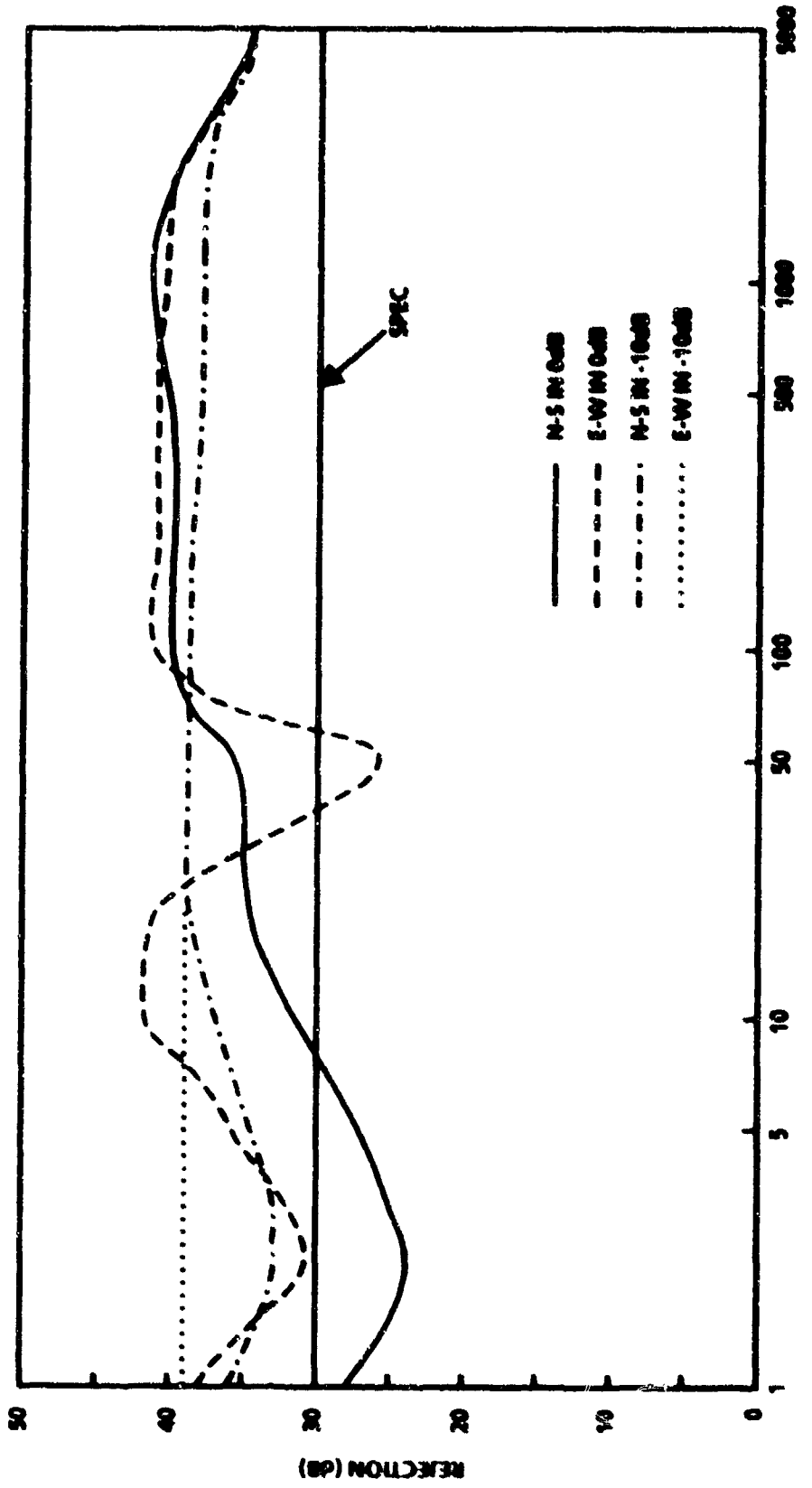


FIGURE 15 DIPOLE CHANNEL SEPARATION

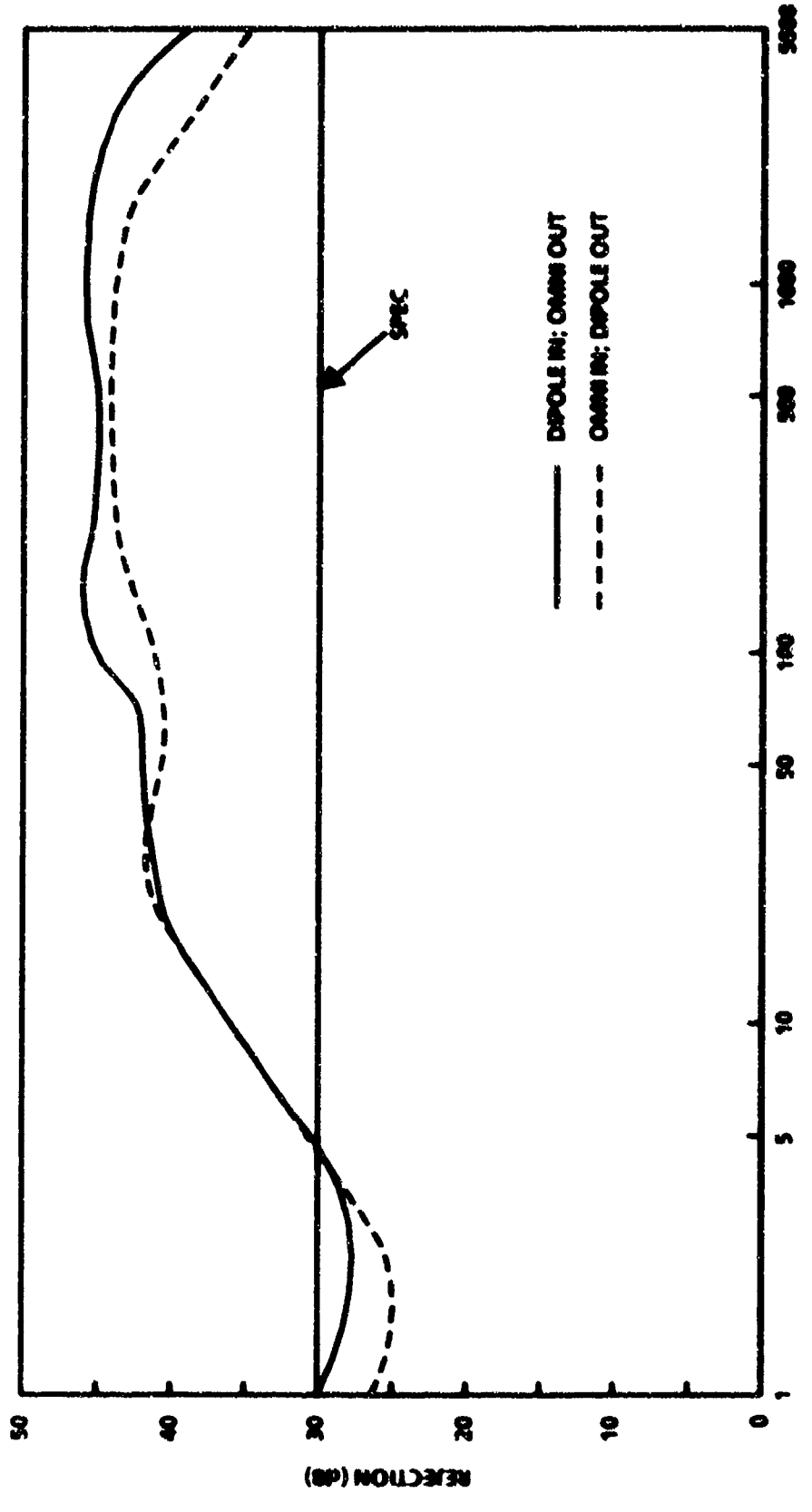


FIGURE 16 DIPOLE-OMNI SEPARATION

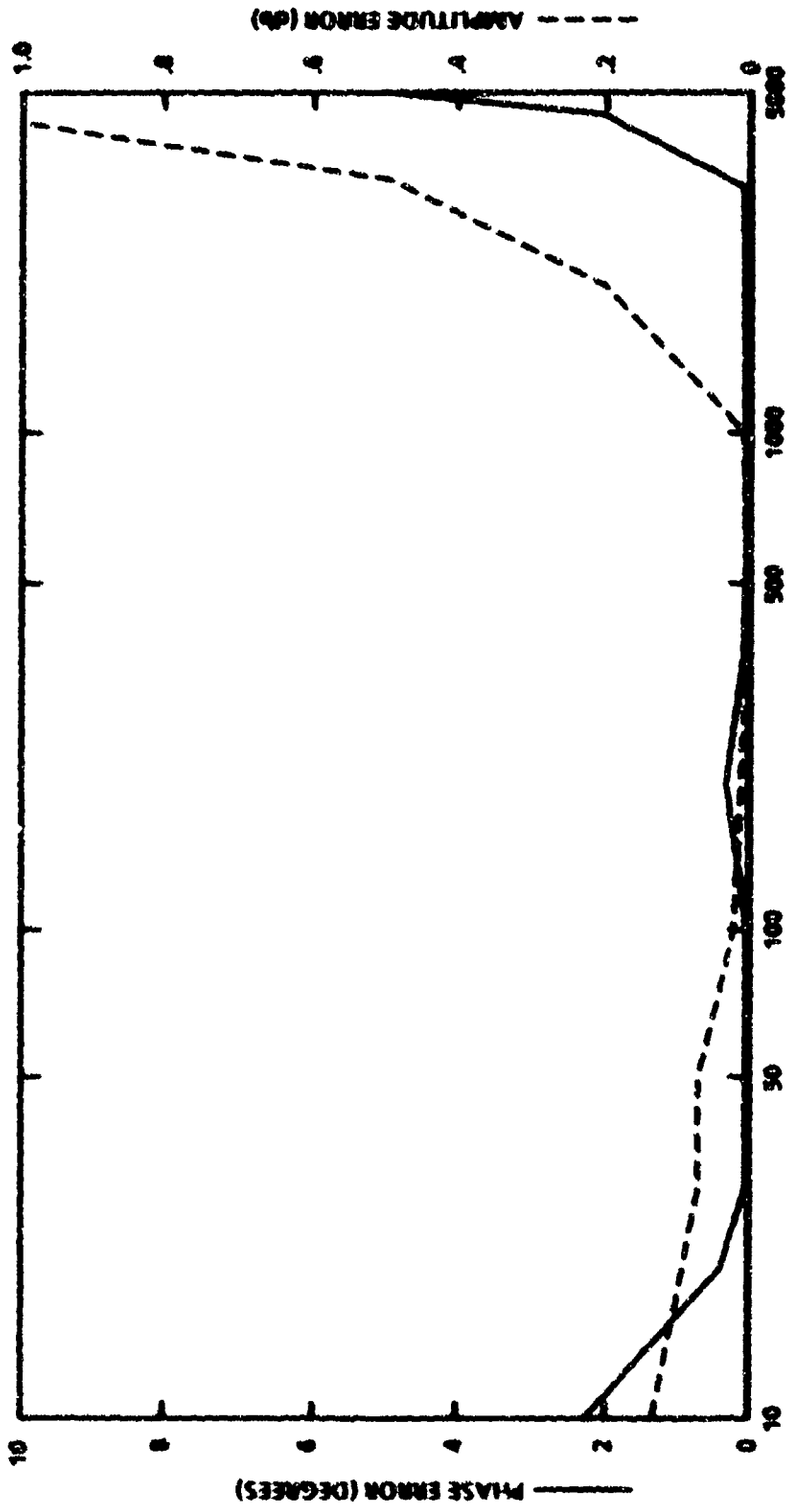


FIGURE 17. N-S TO E-W ERROR

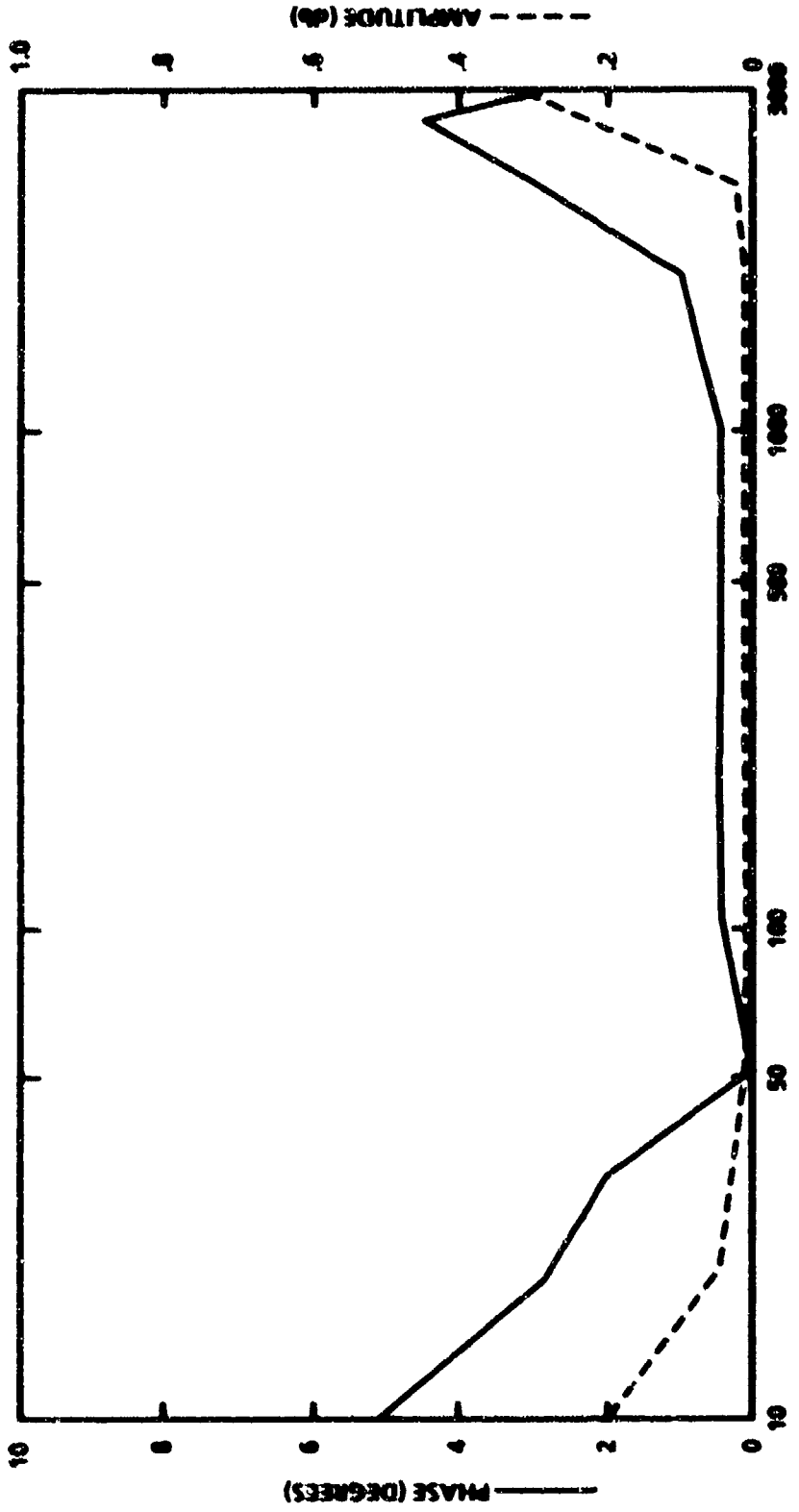


FIGURE 18 N-S TO OMNI ERROR

APPENDIX A

MULTIPLEXER CHECKOUT AND ADJUSTMENT

1. Insert card into rack or test fixture. Make sure supplies are adjusted to ±6V ±15 mV. If supplies cannot be adjusted, recalibrate card with the same supply it is operated with (step 3 primarily).

2. Check oscillator output (pin 20). It should be a square waveform, 0 to +6V, 60.000 kHz ±30 Hz.

3. Set the three inputs pots half way up. Observe the output (pin 2) with no signals in. Ground pins 4 and 8. Adjust the two balance pots alternately for minimum output signal using a filter set at 15 kHz and a true-RMS AC voltmeter, or spectrum analyzer, observing the 15-kHz line.

4. Ground pin 8 only. Output should be 15 kHz ±15 Hz, fairly sinusoidal. Adjust output pot for 100 mVRMS (-20dBV).

5. Ground pin 4 only. Output should be 7.5 kHz ±7.5 Hz, sinusoidal. Amplitude should be about 100 mVRMS. There is no adjustment.

6. Ground pins 4 and 8. Place a 1-kHz, 1-VRMS sine on OMNI in (pin 31). Adjust the corresponding input pot for 0.707 VRMS (-3dBV) at output. Repeat for E-W in (pin 28). On a spectrum analyzer this will be -6dBV lines at 14 kHz and 16 kHz. Repeat for N-S in (pin 34). Place signal on all three inputs. Overload lamp should light.

7. Check frequency response. For each of the three channels, increase input frequency until output level drops 3 dB from that at 1 kHz. Input frequency should be 5 kHz ±0.5 kHz.

8. As a double check, connect the multiplexer to a demultiplexer if available (this step is optional but it may show up problems the calibration procedure does not catch). Place a 1-kHz 1-VRMS (0 dBV) sine wave on the N-S input. Lock lamp should be lit. Overload lamp should be dark. Check to see that the 1-kHz 1-VRMS input signal appears at the N-S output. Move input signal to E-W input and check to see that it appears at the E-W output. Move input signal to OMNI to see that it appears at OMNI output. Output level should be 0 dBV ±0.3 dB for all three cases. Signal on the two unused channels should be below -30 dBV in all cases. Check frequency response for all three channels. It should be down 6 dB at 5 kHz ±0.5 kHz. On the low end it should drop less than 3 dB at 3 Hz. Check feedthrough and noise at the outputs with no signals in. It should be below -50 dBV for each, true RMS.

APPENDIX B

MULTIPLEXER CHECKOUT AND ADJUSTMENT

1. Insert card into rack or test fixture. Make sure supplies are adjusted to ±6V ± 15 mV. If supplies cannot be adjusted, card should be readjusted with the same supply it is operated with (step 3 primarily).

2. Place a 7.5-kHz, 100-mV RMS (-20dBV) sine wave on the input (pin 34). Adjust the pots for 180-degree phase shift through each section. Recheck filter to see that it peaks at 7.5 kHz ±75 Hz.

3. Place a 20-kHz, 1-VRMS (0dBV) sine wave on the input (pin 34). Set the 15-kHz integrator balance pot fully counterclockwise. The output (pin 27) should drift up to about 4.5 V, reset to about +3 V, drift up again, etc. Set the pot fully clockwise. The output should drift down to about 1.5 V, reset to about +3 V, drift down again, etc. Adjust the pot for minimum drift of the 15-kHz integrator by observing the voltage at pin 27 with a voltmeter having at least 1-mV sensitivity.

4. Change input to 1 kHz. Adjust the OMNI pot for 1.4 VRMS (+3 dBV) at OMNI output (pin 24). Lock lamp should not light.

5. Place at the input a composite waveform consisting of a 16-kHz, 0.5-VRMS (-6 dBV) sine wave plus a 7.5-kHz, 0.5-VRMS (-6 dBV) rectangular wave of 75%, 25% duty cycle. Lock lamp should light. Overload lamp should not light. N-S (pin 26) and E-W (pin 22) outputs should be sine waves, 1 kHz. Adjust the dipole pots to give 0.5 VRMS (-6 dBV) at each. Increase the sine wave amplitude 10 dB. Overload lamp should come on.

6. Check the frequency response of the OMNI by inserting the signal of step 4 but increasing the frequency until the OMNI output amplitude drops 3 dB. Frequency should be 5 kHz ±0.5 kHz. Check the frequency response of each dipole by inserting the composite signal of step 5 but increasing the input sine wave frequency until the output amplitude drops 3 dB. Output frequency should be 5 kHz ±0.5 kHz. Check feedthrough and noise by observing the three outputs with no signal into the demultiplexer. It should be below -50 dBV for each, true RMS.

7. As a double check, connect a multiplexer to the demultiplexer if available (this step is optional but it may show up problems the calibration procedure does not catch). Place a 1-kHz, 1-VRMS (0 dBV) sine wave on the N-S input. Lock lamp should light. Overload lamp should not light. Check to see that the 1-kHz, 1-VRMS input signal appears at the N-S output. Move the input signal to the E-W input and check to see that it appears at the E-W output. Move the input signal to OMNI input and check to see that it appears at the OMNI output. Output level should be 0 dBV ±0.3 dB for all three cases. The signal on the two unused channels should be below -30 dBV in all cases. Check the frequency response for all three channels. It should be down 6 dB at 5 kHz ±0.5 kHz. Check feedthrough and noise at the outputs with no signals in. It should be below -50 dBV for each, true RMS.

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This report describes the updated version of a multiplexer-demultiplexer system for DIFAR signals designed by the Naval Surface Warfare Center's Sensors and Electronics Division. Theory, circuitry and performance are provided. This report also serves as a maintenance manual for the systems.

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